KANCHAN MISHRA

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BASICS

Name: Kanchan Mishra
Date of Birth: 20 February, 1985
Gender: Female

STANDARDIZED TEST SCORES

GRE General Test: 1520/1600 (Test date: September 8, 2008)
(Quantitative - 800/800; Verbal - 720/800; Analytical Writing – 5/6)

TOEFL iBT test : 117/120 (Test date: September 21, 2008)
(Reading – 30/30; Listening – 29/30; Speaking – 28/30; Writing – 30/30)

ACADEMIC QUALIFICATION

Bachelor of Technology- Electronics & Communication Engineering (May, 2007).
Indian Institute of Technology (IIT), Guwahati, India.

- Cumulative Performance Index (CPI): 8.73/10.00.
- Department Rank: 3 (Class-size: 43).

All India Senior School Certificate Examination (2003)
Central Board of Secondary Education, New Delhi, india.

- Aggregate Score: 93.8%.
- Topper in North-East Region (8/28 states), India.

All India Secondary School Examination (2001)
Central Board of Secondary Education, New Delhi, india.

- Aggregate Score: 92.4%.
- Topper in North-East Region (8/28 states), India.

WORK EXPERIENCE

NVIDIA GRAPHICS PVT. LTD., BANGALORE, INDIA
ASIC Design Engineer (July, 2007 – till date)

GPU R&D Team: (Nov, 2008 onwards) Research & Development in Peer-2-Peer GPU interactions for SLI technology and GPU memory management system for next generation of NVIDIA GPU architectures.

Memory Controller: (Sept, 2008 –Oct, 2008): For a Single Chip (Northbridge + Southbridge +iGPU) 55nm solution for Penryn based platforms, a low-power refresh of 65nm chipset.

- Technology: DDR2/DDR3 SDRAM.
- Netlist only project.
- ECOs for power and timing fixes/ enhancements.
- Unit and system level directed verification: Writing directed tests for reproducing failures seen on Silicon (in the previous chip revision) in the sims and root-causing them for ECO fix.
- Unit level randoms: Tweak/add randomization parameters to capture/reproduce/verify failures and the fixes.

PCI Express Units: (June-Aug, 2008):For a Southbridge(+iGPU) chipset for Havendale platform.

- Technology: PCIE Gen2.0
- System verification of PCIE based units, viz. DMI(x4), PEG(x16), DSP-TMS(x22), PXB HUB(internal switch between USP-PEG, USP-DMI on chipset and the rest of chipset):
    - Testbench Support: These are completely newly added units and had no testbench support. Task involved building system level API support, multiport BFM wrappers, and multiport APIs. Adding System-level TB support for PCIE based units.
    - Verification: Making Test-plan for the four units, writing system-level directed tests for the features of the four units, debug and Bug tracking through bug reports.

Memory Controller: (Dec, 2007 – May, 2008): For a Single Chip (Northbridge + Southbridge) 65nm solution for Penryn based platforms.

- Technology: DDR2/DDR3 SDRAM.
- RTL Design: Added trimmer support for Quse Fine Delay, Advanced Path checker, modified RTL logic for RCB decoding as per low-end system memory requirements, Updated some of the state machines accordingly.
- Test-bench support:
    - System-level: Updated DIMM models and reverse RCB logic model for new SKU; C++ based algorithms for Read/Write leveling delays; MEM-PLL and wall-clock algorithms. Updated unit and system level monitors, and Memory Performance monitors.
    - Unit-level: Modified API for unit and system level. Updated CPU to memory Driver (BFM) and PMU BFM for memory unit verification. Added RCB test-bench for verifying the new RCB code/decode scheme. Added tests for verifying new features.
    - Verification: Test-plan; Front-end debug at unit and system level. Functional coverage, code coverage, register coverage. Clock Domain Crossing (CDC) check.

Miscellaneous:

- Handy with computer interconnect protocols such as HT3, FSB and CSI and bus interface; Overall Computer Architecture; ATE v2 flow for DFT; Gate level simulations.

RESEARCH INTERNSHIPS

DEPARTMENT OF SIGNALS & COMMUNICATION, ENST-BRETAGNE, FRANCE

Research Intern (May- July, 2006)

- Worked on 'Study & Simulation of Soft-Input Soft-Output MMSE Turbo-Equalizer using Interference Canceller Linear Equalizer and BCH block codes and Convolution codes' on MATLAB and C/C++ platform, under the supervision of Dr. Dominique LeRoux, Asst. Prof, Department of Signals & Communication, ENST-Bretagne, France. Received Research Intern Scholarship from ENST-Bretagne. Received French Government Incentives Scholarship, from French Embassy, India.

BHABA ATOMIC RESEARCH CENTRE, MUMBAI, INDIA

Research Trainee (December, 2004)

- Worked on the 'Software development for a Robotic Cart' under the supervision of Dr. J.K. Mukherjee, Head DRHR, BARC, Mumbai. The work involved development of robotic vision for detection of nuclear material based on sensor data and development of motion controller software which would enable the control of the speed and direction of the cart through multiple computer interfaces and also give a visual display of the cart's motion. The coding was done in VB6 environment.

PROJECT PROFILE

- CPFSK Demodulation Techniques, Supervisor: Prof. A. Mahanta, Dept. of ECE, IIT Guwahati, India, July 2006- April 2007.
- Sub-band coding of Images, Supervisor: Dr. SRM Prasanna, Dept. of ECE, IIT Guwahati, Jan-Apr, 2007.
- A survey of contemporary Medical Image Compression Techniques, Supervisor: Prof. P.K. Bora, Dept. of ECE, IIT Guwahati, July-Nov, 2006.
- Design and Implementation of a WLAN system, Supervisor: Dr. K.R. Singh, Dept. of ECE, IIT Guwahati, India, Jul- Nov, 2006
- Design of a Compact PIFA for PCS Applications, Supervisor: Dr. K.R. Singh, Dept. of ECE, IIT Guwahati, India, Jan- Apr, 2006
- Hardware Implementation of a Speech Codec, Supervisor: Dr. A. Mitra, Dept. of ECE, IIT Guwahati, India, Jan- Apr, 2006.

- Gabor filter based VOP detection algorithm, Supervisor: Dr. SRM. Prasanna, Dept. of ECE, IIT Guwahati, India, May- Jul, 2005.
- Development of an Education Kit for a basic course in Communications, Supervisor: Dr. SRM. Prasanna, Dept. of ECE, IIT Guwahati, India, Jan- Apr, 2005.
- Design & Construction of a Tachometer, Supervisor: Prof. A.K. Gogoi, Dept. of ECE, IIT Guwahati, India, Jul- Nov, 2004.

Please visit my web page for detailed project profile: http://kanchan-iitg.tripod.com/

ORAL PRESENTATIONS

- Ferro-electric materials in Micro-electronics, at Indo-German Winter Academy, Dec-2005.
- Sub-band coding of images, IIT Guwahati.
- A survey of contemporary Medical Image Compression Techniques, IIT Guwahati.
- Fundamentals of Turbo-codes, IIT Guwahati, India.
- Study & Simulation of Soft-Input Soft-Output MMSE Turbo-Equalizer using Interference Canceller Linear Equalizer and BCH block codes and Convolution codes, ENST-Bretagne, France.
- Design of a compact PIFA for PCS Applications, IIT Guwahati.
- Hardware Implementation of Speech Encryptor & Decryptor, IIT Guwahati.

SCHOLARSHIPS & HONORS

- French Government Incentives Scholarship for pursuing research internship at ENST-Bretagne, France
  (May-July, 2006).
- ENST- Bretagne Research Intern Scholarship (May-July, 2006).
- Williamson Magor Scholarship (2005-2007)- complete tuition fees coverage of B.Tech.
- Institute Merit Scholarship for being department topper (2003-2004).
- Invited by MHRD to meet **President of India** at the Republic Day (26 January, 2004) as a recognition of my performance in Class-XII (AISSCE-2003).
- Merit Scholarship by Govt. of Assam (India), for performance in Class-XII (2003).
- National Merit Scholarship, Govt. of India for School/ University Toppers (2003).
- Awarded certificate of merit in English for being amongst top 0.1% successful candidates in AISSCE-2003 and AISSE-2001.